would vary widely and would not have the constant resistance of a resistor. Therefore, it would not have been obvious to one of skill in the art to substitute a resistor for a transistor based on the purported functional equivalence shown in Sasaki. The Examiner asserted that FIG. 4(c) of Sasaki showed that a resistor was a functional equivalent to a transistor and that no evidence had been placed in the record to overcome this assertion. However, no agreement was reached.

Claim rejection under 35 U.S.C. §103

The Examiner rejected Claims 1-10 under 35 U.S.C. § 103(a) as being unpatentable over Zhang (USP 6,313,696), in view of Sasaki (USP 5,039,873). While the Examiner did not specifically cite Stockstad (USP 6,429,685) in the rejection, the Examiner also referred to Stockstad in the text that followed the rejection.

In supporting the rejection, the Examiner has asserted several propositions that applicant summarizes as follows: (1) Zhang, FIG. 2, discloses all of the elements recited in Claim 1 except for the bias circuit comprising four resistors, rather than the four transistors shown in Zhang; (2) Sasaki "teaches that when a transistor is on, it is functionally equivalent to a resistor" (referring to FIG. 4(c) and Col. 1, lines 21-22); and (3) The gates of the biasing transistors disclosed in Zhang are tied to a fixed voltage so that the transistors will remain "on." Based on these assertions the Examiner stated that "it would have been obvious to one having ordinary skill in the art at the time the invention was made to substitute a resistor for each of the [biasing] transistors ... in Figure 2 of the Zhang reference because they are functionally equivalent and because it is well known in the art that the impedance of the passive resistor is inherently linear...."

Applicant traverses the rejection for the following reasons: (1) The rejection relies on a suggestion that an always-on field effect transistor is equivalent to a resistor. However, a Rejection may not rely on mere functional or mechanical equivalence to support an obviousness rejection; (2) In the operating environment of the claimed amplifier, a resistor is simply *not* a

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valid equivalent to a field effect transistor; and (3) The fact that references *can* be combined is not sufficient to establish obviousness. These reasons will be argued more fully below.

1.   The rejection applies an incorrect standard in relying on mere functional or mechanical equivalence to support an obviousness rejection.

In rejecting the claims, the Examiner states that Sasaki shows functional equivalence between an always-on FET and a resistor and relies on this alleged equivalence to support the rejection. However, the Examiner has applied an incorrect standard and may not rely on mere functional equivalence. "In order to rely on equivalence as a rationale supporting an obviousness rejection, the equivalency ... cannot be based on ... the mere fact that the components at issue are functional or mechanical equivalents." MPEP § 2144.06, *see also, In re Scott*, 323 F.2d 1016 (CCPA 1963). "[T]o establish obviousness based on a combination of the elements disclosed in the prior art, there must be some motivation, suggestion or teaching of the desirability of making the specific combination that was made by the applicant." *In re Kotzab*, 217 F.3d 1365, 1369 (Fed.Cir. 2000), *see also* MPEP § 2143.01

In the first Office Action (mailed August 28, 2002), the Examiner asserted as the basis for combining the teaching of Zhang with Sasaki was that "it would have been obvious to one having an ordinary skill in the art ... to substitute a resistor for each of the transistors 32, 33, 36 and 37 in Figure 2 of the Zhang reference because they are functionally equivalent." [1st Office Action, p. 4]. In Applicant's "Amendment and Response to First Office Action" (dated January 8, 2003), Applicant traversed the rejection and specifically requested "the Examiner point out the required suggestion to combine." [1/8/2003 Response, p. 5]. In the Second Office Action (mailed April 21, 2003), the Examiner responded by, once again, asserting that "it is obvious to one having an ordinary skill in the art ... to replace each of the transistors 32, 33, 36 and 37 with a resistor because they are functionally equivalent." [2nd Office Action, p. 8]. While the Examiner indicated a mere functional equivalence between a field effect transistor (FET) and a resistor, he did not provide any indication of a suggestion or motivation to combine the references. In response, Applicant filed an RCE on September 19, 2003, in which Applicant once again traversed the rejection and requested that the Examiner present evidence showing a

teaching, suggestion or incentive supporting the combination of Zhang and Sasaki. [9/19/2003 Response, p. 4]. The Examiner issued the present Office Action on October 16, 2003, and stated "it is obvious to one having an ordinary skill in the art ... to replace each of the transistors 32, 33, 36 and 37 with a resistor because they are functionally equivalent." The Examiner also recognized "the advantage of using [a] passive resistor because the impedance of [a] passive resistor inherently is linear." [3rd Office Action, p. 10]. While, with hindsight, the Examiner recognizes the advantage of the invention, the Examiner has made no statement showing a teaching, suggestion or motivation to combine the Sasaki and Zhang references.

Even assuming, *arguendo*, that a resistor is a functional equivalent to a FET[1], the assertion that they are equivalent is simply not enough to sustain an obviousness rejection under MPEP §§ 2143.01, 2144.06. The Examiner must also provide some suggestion or motivation to combine the references. Despite repeated requests, the Examiner has not done this.

2.   In the operating environment of the claimed amplifier, a resistor is simply *not* a valid equivalent to a field effect transistor.

The Examiner bases the rejection on the assertion that a resistor is equivalent to a field effect transistor (FET). However, as applied to a differential amplifier, a resistor is not a functional equivalent to a FET.

The fundamental premise of the rejection was that FIG. 4(c) of Sasaki indicates that a resistor is equivalent to a field effect transistor in the "on" state. However, this fundamental premise is incorrect. Sasaki does not teach that a resistor is a functional equivalent to an always-on FET, but only that an always-on FET can be modeled as a resistor under certain conditions. In the environment of the amplifier disclosed in Zhang, a transistor would *not* act in the same way that a passive resistor would. Thus, as will be shown below, the equivalence model shown in FIG. 4(c) of Sasaki is *not* a correct model for differential amplifiers. Therefore, one of

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[1] Which Applicant disputes.

ordinary skill would *not* have recognized a resistor to be an equivalent to a transistor as a biasing element in a differential amplifier, as claimed in the present application.

A.   Technical Background

As is generally known to those of skill in the electrical arts, the resistance of a resistor is constant over the normal operating range of voltages applied to the resistor. According to Ohm's law, the voltage (V_R) across a passive resistor is proportional to the resistance (R) of the resistor times the current (I_R) flowing through the resistor. Thus, one can determine the resistance of the resistor according to the following formula: $R = V_R \div I_R$. Given the constant resistance of a resistor, the current flowing through a resistor will always be directly and inversely proportional to the voltage. Thus, a curve relating resistor current (I_R) to resistor voltage (V_R) for a resistor would start at the origin of the current-voltage curve and be a straight line for all of the normal operating range of the ideal resistor, with the resistance being equal to the slope of the line and a curve of the resistance (R) of a resistor is always a flat horizontal line (as shown in Exhibit A).

A resistance curve for a FET is different. The current (I_D) flowing through the drain of a FET is a non-linear function of the drain-to-source voltage (V_{DS}) and the gate-to-source voltage (V_{GS}) of the FET. This functional relationship is shown graphically in Exhibit B, p. 313, Fig. 8.15. Exhibit B is a relevant excerpt taken from Sedra and Smith: Micro-Electronic Circuits (which is one of the most highly used texts used to teach upper-level microelectronic circuit analysis courses in the electrical engineering curricula of major universities throughout the world). Exhibit B shows that in a FET, a plot of I_D versus V_{DS} gives rise to a plurality of curves, one for each value of V_{GS}.

As demonstrated in Exhibit C, if V_G is held constant in the always "on" state (as in the biasing transistors of Zhang) and the source is allowed to vary, then the value of V_{GS} will also vary between a maximum level when V_S is at a minimum to a minimum level when V_S is at a maximum. V_{DS} will vary in a corresponding manner. As V_{GS} varies, the I_D-V_{DS} curve for the transistor will change in a non-linear manner as different I_D-V_{DS} curves (each reflecting a

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different value of V_{GS}) are applied. Thus, the resistance of the transistor will also vary. Therefore, if the source voltage of a transistor varies and the gate voltage is held constant, then the transistor is <u>not</u> correctly modeled as a resistor, which has a horizontally flat resistance model.

The equivalence model of Sasaki is merely an approximation that is valid only when V_{GS} is held constant and V_{DS} is allowed to vary only slightly or not at all. In such a situation, the resistance remains approximately constant and resembles the resistance curve of a resistor. On the other hand if the source voltage V_S varies, then the I_D versus V_{DS} curve changes in a dramatically non-straight line manner and, thus, the resistance of the FET varies in a clearly non-linear manner. Therefore, if the operating environment of a FET with a gate tied to a voltage includes a source voltage that varies over any appreciable range, then the FET will exhibit a varying resistance and is not properly modeled as a passive resistor.

B.   Application to Rejection

The FET-resistor equivalence model shown in FIG. 4(c) of the Sasaki reference is valid *only* when a FET is operating with a gate-to-source voltage (V_{GS}) that is held constant, and then it is a useful model *only* so long as the drain-to-source voltage (V_{DS}) is maintained within a narrow range. However, as will be demonstrated below, the biasing FETs employed in Zhang have widely varying source voltages and, thus, widely varying V_{GS}. Therefore, a resistor is <u>not</u> a functional equivalent of a FET when used as a biasing transistor in a differential amplifier.

It is important to remember that the Sasaki model is presented in the context of a microwave switched line phase shifter. [Sasaki, Col. 1, lines 5-10]   The incompleteness of the Sasaki equivalence model of FIG. 4(c) may be insignificant in the context of a microwave switched line phase shifter as shown in Sasaki. This is because the approximation of FIG. 4(c) applies only when the FET is held in an "on" state [Sasaki, Col. 1, lines 20-22], in which a constant V_{GS} (e.g., -5V) is applied to the FET [Sasaki, Col. 1, lines 26-31]. Given that a microwave RF signal is then transmitted through the FET, one can assume that the source to

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drain voltage (e.g., the voltage between node 1 and node 2 in FIG. 4(a)) would be essentially constant. Otherwise, the varying resistance (and, thus, the varying impedance) resulting from a varying V_{DS} would result in distortion of the RF signal being switched by the circuit. Thus, FIG. 4(c) shows an approximate equivalence between a FET and a resistor only in the special case when the V_{GS} and V_{DS} of the FET are held at an essentially constant value. Therefore, the equivalence model shown in Sasaki, FIG. 4(c), is not a useful approximation when V_S is likely to vary.

The Examiner cited Stockstad. However, Stockstad supports Applicant's argument for non-equivalence, rather that the equivalence asserted in the Office Action. Stockstad indicates that a transistor is not an equivalent to a resistor because of "the inherent non-linearity of the output impedance of a transistor," but that "[t]he impedance of a passive resistor is inherently linear...." [Stockstad, Col. 5, lines 19-20]. Thus, Stockstad serves only to further contrast a FET from a linear resistor and demonstrates the inadequacy of the equivalence model disclosed in Sasaki.

Unlike the circuit in Sasaki, the biasing transistors shown in FIG. 2 of Zhang (32, 33, 35 and 37) are likely to have a source voltage (V_S) that varies significantly. While the gate voltages of these transistors are tied either to V_{dd} or to Ground, the source voltages are coupled to nodes that have voltages that will vary from near ground to near V_{dd} (Col. 7, lines 12-15). Because the source voltages vary significantly and the gate voltages are held constant, V_{GS} for these transistors varies significantly during normal operation. Thus, the resistance of these transistors would also vary significantly, in contrast to the resistance of a passive resistor, as claimed. For example, as shown in Exhibit C, when V_S is at its minimum (A), the values of both V_{DS} and V_{GS} both are at their maximum, and the I_D/V_{DS} curve of the FET is the top curve and the FET is operating in the saturation mode. On the other hand, as V_S goes to its maximum, the values of both V_{DS} and V_{GS} go to their minimum and the I_D/V_{DS} curve is the bottom curve. The operating point on each of these curves gives the resistance shown by the FET for the given value of V_S, which clearly varies as a function of V_S.

The analysis performed by Mr. Preuss confirms this. (A copy of the relevant curves[2] is shown in Exhibit D for the convenience of the Examiner.) In Fig. 2 of the Preuss Submission, the dotted line is a graph of the source-drain resistance of a biasing FET (Item No. 36 shown in FIG. 2 of Zhang, *see also*, ¶ 8 of the Preuss § 1.132 Affidavit) during normal operating conditions of the Zhang amplifier. The solid line is a graph of the resistance of a resistor put in place of this FET. The inputs and outputs used in this simulation are shown in FIG. 3 of Attachment C, where input INP corresponds to "ina" of Zhang and INM corresponds to "inb" of Zhang (item nos. 10 and 12 in FIG. 2, respectively). As is clearly shown in the Preuss simulation, a value in which "ina" is low and "inb" is high causes the resistance of FET 36 to be virtually 0 Ohms. When "ina" is high and "inb" is low for a relatively long period of time, the resistance of FET 36 goes up to its maximum resistance. If this situation lasts for a relatively shorter period of time, the resistance never reaches its maximum resistance. In stark contrast, the resistance curve of a similarly placed passive resistor is flat throughout the simulation. This clearly shows that the relevant transistors from FIG. 2 of the Zhang reference do **not** behave linearly, as do passive resistors. Therefore, a resistor (which has a flat resistance curve) is **not** a functional equivalent to a transistor that is used to bias an amplifier (which has a varying resistance curve). Therefore, it would **not** have been obvious to one of skill in the art to combine the resistor shown in Sasaki with the amplifier shown in Zhang to achieve the claimed invention.

Furthermore, the Sasaki equivalence model makes no mention of any capacitance in the FET. For the equivalence model of Sasaki to be correct, a FET in the "on" state would have a capacitance equal to that of a resistor, which is clearly not true when applied to an amplifier. A correct FET model showing capacitance is shown in Exhibit E, a relevant excerpt taken from Hodges and Jackson: <u>Analysis and Design of Digital Integrated Circuits</u> (which is a standard text used to teach graduate level transistor analysis courses in electrical engineering at many major universities). A FET, even in the always "on" state exhibits the following capacitances: gate-to-drain; gate-to-source; gate-to-base; drain-to-base; and source-to-base. [Exhibit E, Figure 2.6, p.

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[2] Additional labeling has been applied to the curves shown in Exhibit E to improve clarity. Applicant hereby asserts that the curves themselves are identical to the curves submitted with the

53 – the most complete model for a FET is shown in Figure 2.8, p. 57]. These capacitances can introduce significant cumulative time delays in a dynamic circuit (as has been shown previously in the analysis performed by Mr. Preuss [Submission filed 9/19/2003]). While the FET capacitances may be insignificant in the circuit disclosed Sasaki, they introduce important delays in a differential amplifier, as claimed in the present application. (The present application explicitly states that "resistors have approximately one tenth the capacitance of a transistor gate of similar size." [*See*, Present Application, p.5, lines 5-6]. It is the decreased capacitance of the present invention that gives rise to the improvements shown in the Preuss analysis.

Because the resistance model shown in FIG. 4(c) of Sasaki is not a valid resistance model in the operating range of a FET used in the amplifier of Zhang and because the model shown in FIG. 4(c) of Sasaki does not include the capacitances that are significant in the amplifier disclosed in Zhang, the equivalence model shown in FIG. 4(c) of Sasaki is *not* valid in the context of the amplifier shown in Zhang. Therefore, one of ordinary skill in the art would not recognize any equivalence between a linear resistor and a biasing FET and, therefore, one of ordinary skill in the art would have no motivation to combine Zhang with Sasaki to achieve the invention claimed in the present application. For this reason, Applicant believes that the rejection has been overcome and respectfully requests that it be withdrawn.

3.   The fact that references *can* be combined is not sufficient to establish obviousness.

None of the office actions include any indication that there is a suggestion of the desirability to combine the Sasaki reference with the Zhang reference. "The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination." MPEP §2143.01 Before the PTO may combine the disclosures of two or more prior art references in order to establish *prima facie* obviousness, there must be some suggestion for doing so, found either in the

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§ 1.132 Affidavit filed on September 19, 2003. The original of this figure is found at submission filed 9/19/2003, Attachment C, Fig. 2

references themselves or in the knowledge generally available to one of ordinary skill in the art. *In re Jones*, 958 F.2d 347, 351 (Fed.Cir. 1992).

None of the references state that a field effect transistor (FET) can be replaced by a resistor. The Sasaki reference indicates only that, in a configuration of a FET in which the gate is tied to a voltage such that it is in the always "on" state, a FET can be modeled as a resistor. Nothing in Sasaki, or the general knowledge of the art, teaches or suggests replacing a FET with a passive resistor.

Most if not all inventions arise from a combination of old elements. *See In re Rouffet*, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457 (Fed.Cir.1998). Thus, every element of a claimed invention may often be found in the prior art. However, identification in the prior art of each individual part claimed is insufficient to defeat patentability of the whole claimed invention. *See id.* Rather, to establish obviousness based on a combination of the elements disclosed in the prior art, there must be some motivation, suggestion or teaching of the desirability of making the specific combination that was made by the applicant. *In re KOTZAB*, 217 F.3d 1365, 1369 (Fed.Cir. 2000). The Examiner must provide particular findings related thereto. "Broad conclusory statements standing alone are not 'evidence.'" *Id.*

While not explicated stated in the record, the Examiner implies that it is well known that an always-on FET is the same as a resistor and, for that reason, there was a motivation to combine Sasaki with Zhang. Pursuant to MPEP § 2144.03(C), Applicant hereby challenges this assertion as not properly based upon common knowledge and hereby respectfully requests that the Examiner provide documentary evidence that shows a teaching, suggestion or motivation to combine the cited references.
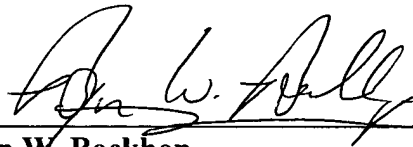
If no documentary evidence sufficient to meet the requirements of MPEP § 2144.03(C) is provided, then Applicant believes that for the reason that there is no teaching, suggestion or motivation to combine Sasaki with Zhang, this rejection has been overcome and respectfully requests that it be withdrawn.

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CONCLUSION

Applicant believes that the remaining § 103(a) rejection has been overcome for three reasons, any one of which would be sufficient *by itself* to overcome the rejection. Therefore, Applicant requests that all claims be allowed.

No additional fees are believed due. However, the Commissioner is hereby authorized to charge any additional fees which may be required, including any necessary extensions of time, which are hereby requested, to Deposit Account No. 502666.
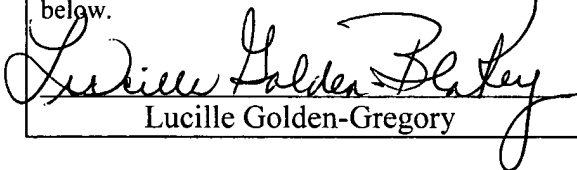
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